# Semiconductor nanowire devices

**For the past ten years the idea of using self-assembled nanostructures to overcome the limitations of top-down fabrication has been the driving force behind the tremendous interest in semiconducting nanowires and nanotubes. However, it has become clear that the engineering issues associated with bottom-up technology using self-assembled nanowires and nanotubes remain challenging.**

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**With the great advances in synthesizing nanowires with unique axial and radial heterostructures, an increasing number of research groups are demonstrating that nanowires are suitable for investigating novel nanoscale physics; this work also guides industry by providing early and crucial insights into device behavior at sub-lithographic length scales. For example, major stakeholders in Complementary Metal-Oxide-Semiconductor CMOS technology are incorporating the nanowire Field-Effect Transistor (FET) concept into post-CMOS processes and have demonstrated substantial advantages. Beyond FETs, new and exciting applications for nanowire memory based on phase change show potential for studying fundamental memory switching at sub-50 nm length scales where the top-down approach tends to damage the materials. Here, we review the most recent progress in both bottom-up and top-down nanowire research for electronic applications.**

## The beauty of being small and complex

It is widely agreed that new materials, structures and device concepts are needed to sustain the relentless trend of transistor scaling that is required for continued progress in CMOS development. Perhaps the most prominent materials/structures being considered are semiconductor nanowires, which are single crystals with diameters of a few nanometers and lengths up to tens of micrometers[1–5]. A typical 'bottom-up' nanowire synthesis process involves Vapor–Liquid–Solid (VLS) or vapor–solid growth mechanisms in which nanoparticles are used as catalysts to continuously feed the one-dimensional (1-D) material growth[1–5]. The beauty of this approach lies in the ability to grow a wide range of nanowire materials, including group IV, III–V and II–VI core/shell, superlattice and branched structures, while simultaneously allowing precise control of the nanowire composition, morphology and electrical properties through fine tuning of growth parameters that enhance or suppress the axial and radial growth processes[1–4] (Fig. 1).

A large number of studies have explored nanowires as new building blocks in electronics[6–8], photonics[9,10], biochemical[11,12] and chemical sensors.[13–16] The most commonly cited properties in these studies originate from the small diameters, large surface areas and relatively smooth surfaces of nanowire materials that may be difficult to obtain from their 'top-down' aggressively scaled counterparts.



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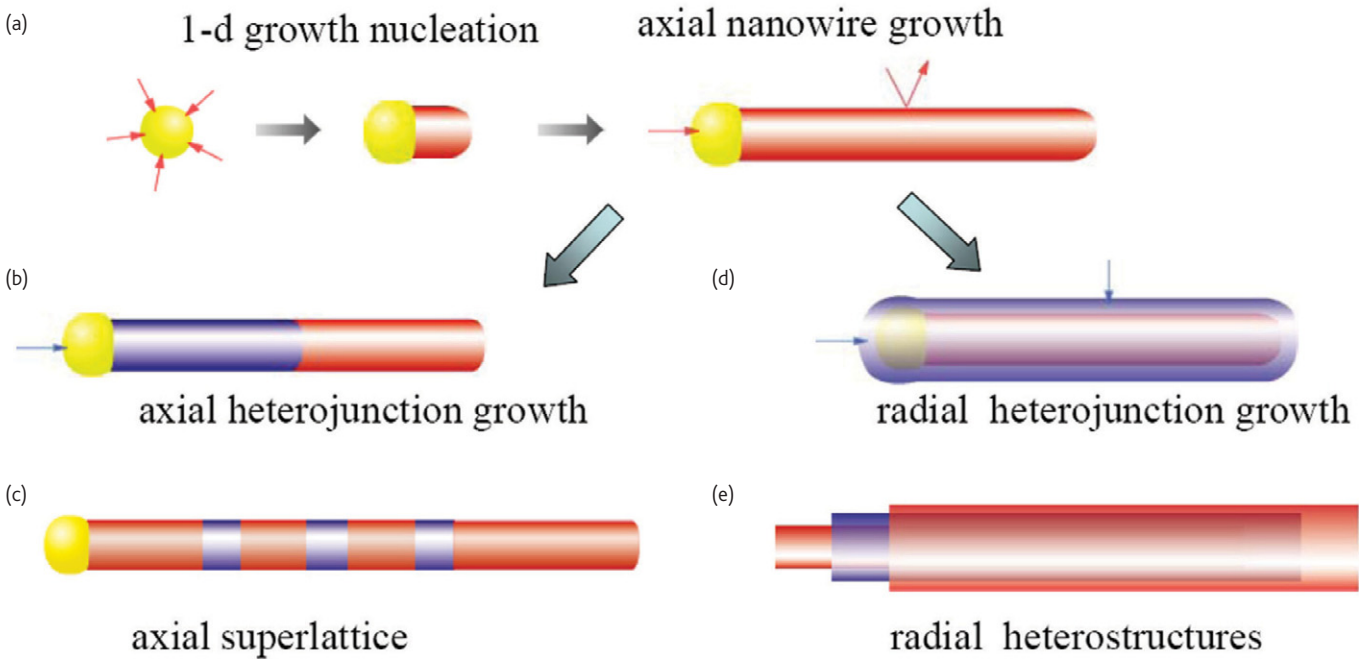


*Fig. 1 Schematic of nanowire and nanowire heterostructure growth. (a) Nanowire synthesis through catalyst-mediated axial growth. (b,c) Switching of the source material results in nanowire axial heterostructures and superlattices. (d,e) Conformal deposition of different materials leads to the formation of core/shell and core/multishell radial nanowire heterostructures.*

In addition, one aspect that truly sets the 'bottom-up' nanowire system apart is the ability to obtain heterostructures during growth, including radial core/shell heterostructures and axial superlattice heterostructures (Fig. 1) that are very challenging to match, or are even unobtainable, via top-down lithographic means. For example, a Ge/Si core/shell nanowire heterostructure can be obtained by the conformal growth of a Si shell over a suspended Ge nanowire core inside the same growth chamber without breaking vacuum[17,18]. Due to the large valence band offset and Fermi level pinning between Ge and Si, a 1-D hole gas can be formed and confined inside the Ge core even with intrinsic core and shell materials[18]. Similar bandstructure engineering techniques have been widely used in planar systems to produce high-mobility two-dimensional electron and hole gases[19, 20]. Furthermore, the small size and volumetric similarity in the core and shell of the nanowire heterostructure system can lead to coherently strained heterostructures free from interfacial dislocations even for materials with relatively large lattice mismatch (e.g. Ge and Si) – a feat that is obviously desirable but fundamentally prohibited in planar structures[21–23].

Compared with homogeneous Si or Ge nanowires, the Ge/Si core shell heterostructure nanowires offer two key advantages: first, transparent (negative Schottky) contacts to the conduction channel can be formed due to the alignment of the energy bands; second, impurity and surface scattering can be suppressed by the elimination of dopants in the channel and surface passivation provided by the shell layer. These two factors have led to the successful demonstration of ultrahigh-performance p-type transistor devices by the Lieber group at Harvard[6,24] (Fig. 2). For example, using the intrinsic gate delay CV/I as the benchmark, operating speeds of up to 2 THz have been suggested for Ge/Si nanowire FETs with 40 nm channel length and $HfO_2$ gate dielectric[24]. The scaling potential of the transistor devices using the CV/I benchmark has also been shown to be superior for the Ge/Si core/shell nanowires compared with their planar counterparts[6,24]. Furthermore, the clean 1-D hole gas system is a unique platform with which to study the rich quantum phenomena in 1-D systems that include coupled quantum dots and tuneable Josephson junction devices[6,18,25,26]. Similarly, 1-D electron gas systems have been demonstrated by exploring the conduction band offset in core/shell nanowire heterostructures that include GaN/AlN/AlGaN and InAs/InP nanowire heterostructures that exhibit electron mobilities as high as 3100 and 11500 $cm^2/V{\cdot}s$ at room temperature, respectively[27,28]. Studies on prototype n-FET devices based on the GaN/AlN/AlGaN system with 1 μm channel length and $ZrO_2$ gate dielectric showed on-currents of 500 mA/mm, subthreshold slopes of 68 mV/decade, and an on/off current ratio of $10^7$[7,28]. In another spectacular display of the flexibility and controllability of the bottom-up nanowire system, efficient, multicolor Light-Emitting Diodes (LEDs) were demonstrated in n-GaN/$In_xGa_{1-x}N$/i-GaN/p-AlGaN/p-GaN core/multishell devices (Fig. 3), in which the radiative recombination and photon confinement occur at the $In_xGa_{1-x}N$ shell layer, and the wavelength of the emitted light can be systematically adjusted from 367 to 577 nm by tuning the In concentration during nanowire growth[5,29].

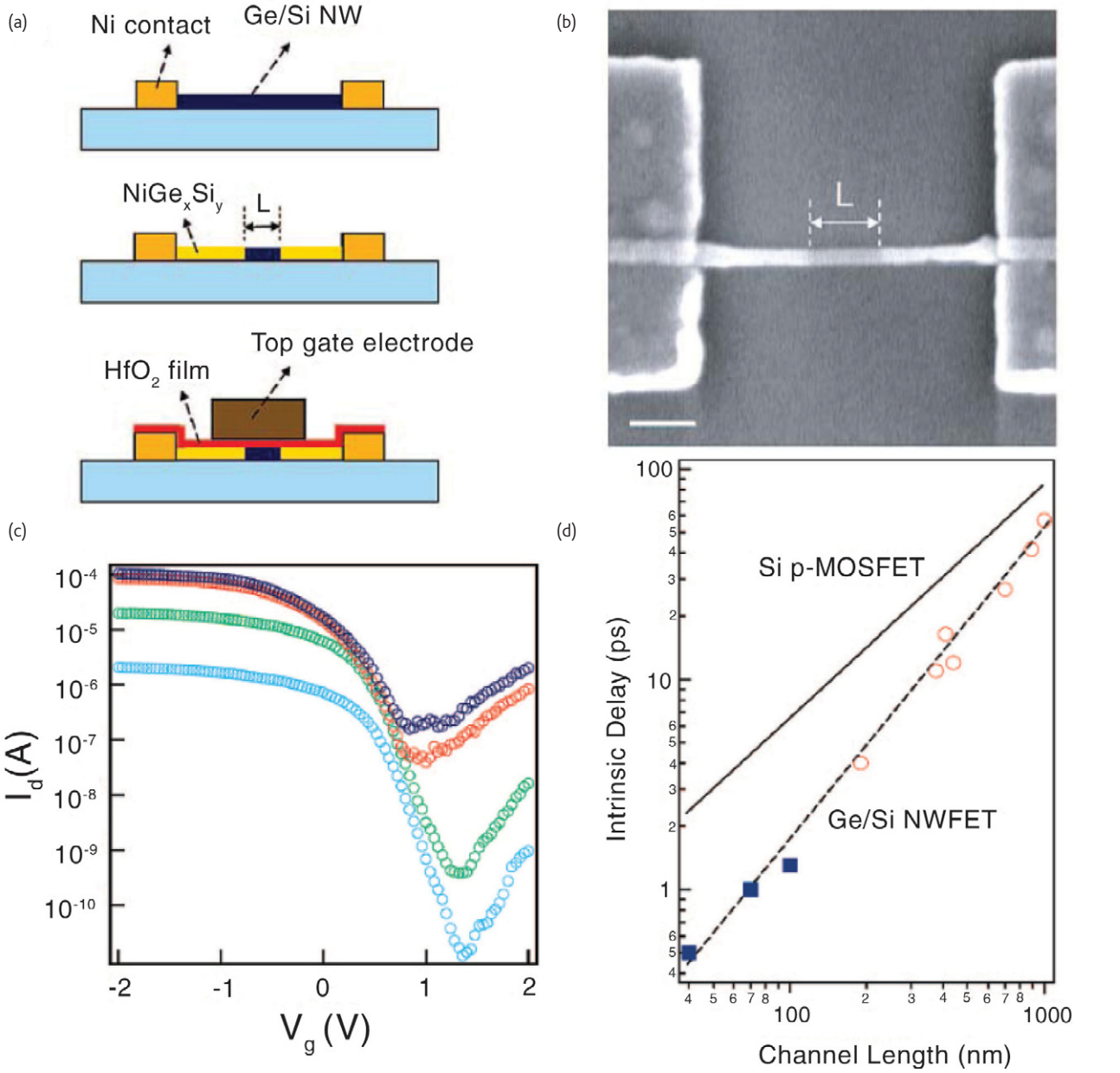


*Fig. 2 High-performance Ge/Si core/shell nanowire FETs. (a) Schematic of the nanowire FET showing integrated nanoscale silicide source/drain electrodes and top-gate structure. (b) Scanning electron microscope image of a device prior to gate and dielectric deposition. Scale bar: 500 nm. (c) Transport data from a 100 nm channel length device, with cyan, green, red, and dark blue data corresponding to Vds = -10 mV and -0.1, -0.5, and -0.8 V, respectively. (d) Length dependence of intrinsic delay CV/I and compared with Si p-MOSFET results. Reproduced with the permission from Hu et al.[24], © 2008 American Chemical Society.*

Another area in which nanowire research may have a significant impact is flexible and/or transparent electronics that need to be built on non conventional substrates such as plastics and glass. Traditionally, the performances of such Thin-Film Transistor (TFT) devices are limited[30] (mobilities ~ 1 cm$^2$/V·s) since the low thermal budget imposed by the glass or plastic substrates presents a significant challenge for high-quality material growth. In the nanowire TFT approach, instead of directly growing crystalline materials on plastic or glass, the thermal budget problem is circumvented by transferring the nanowires from the growth substrate to a separate device substrate, thus decoupling the high-temperature processes required for high-quality material growth from the low-temperature processes required by device fabrication on non conventional substrates. These applications are particularly suitable for nanowire electronics since (a) a wide range of high-quality nanowire materials are available; (b) efficient assembly techniques that provide position registry at the individual nanowire level are elusive but a variety of techniques have been developed to produce aligned nanowire films[31]; and (c) the

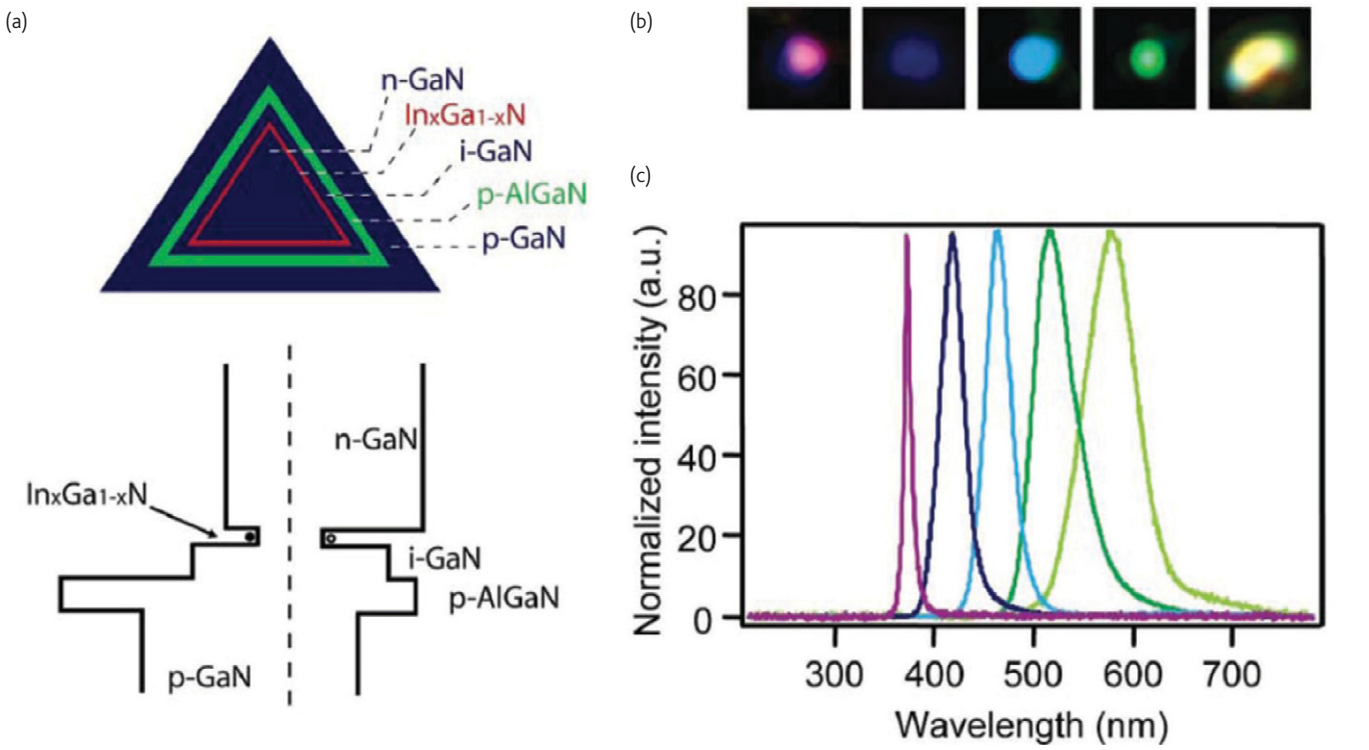


*Fig. 3 Nanowire core/multishell LEDs. (a) Schematic of the core/multishell cross-section and energy band line-up. (b) Optical microscopy images collected from around the p-contact of nanowire LEDs in forward bias, showing purple, blue, greenish-blue, green and yellow emission, respectively. (c) Normalized electron-luminance spectra recorded from five representative forward-biased multicolor nanowire LEDs. Reproduced with the permission from Qian et al.[5], © 2005 American Chemical Society.*

fabrication and operation of the nanowire TFTs are fairly insensitive to the device substrates being used. Using the nanowire TFT approach, small-scale integrated circuits such as ring-oscillators with operating frequencies of 11.7 MHz and AC inverters with operating frequencies of 50 MHz have been demonstrated on glass and plastic (Kapton) substrates, respectively[32,33]. In addition, transparent nanowire TFTs with transmittances of ~80% and operating frequencies above 100 MHz have also been demonstrated[34,35]. Significantly, our DC and radio frequency characterizations show that nanowire-based TFTs exhibit tightly distributed performance metrics that are insensitive to nanowire density fluctuations[34,35]. Device measurements and finite-element simulations also show that for devices using 130 nm thick $SiO_2$ as the gate dielectric, the gate capacitance $C_g$ reaches 90% of that expected for a continuous film if the nanowire coverage is >25% and is insensitive to nanowire densities above this threshold (Fig. 4d)[35]. The physical origin of this capacitance saturation effect is that above a certain threshold the nanowire array can efficiently screen the field lines from the gate and acts effectively as a continuous film. Since the TFT device parameters such as drain current ($I_{ds}$) and transconductance ($g_m$) are directly related to $C_g$, fluctuations in the nanowire densities will thus have little effect on the TFT performance beyond this threshold. For devices with thinner gate oxide, a tighter tolerance is expected, but our calculations have shown that even for nanowire TFTs with 10 nm gate oxide, variations in nanowire density by ±10% will only lead to ±5% fluctuation in performance if the nanowire coverage is >75%. These observations have to a large extent addressed the uniformity question regarding nanowire TFT-based electronics since a number of assembly techniques can be used to obtain nanowire films with high surface coverage including the close-packed form with a coverage of ~100%[31]. Considering these factors, it is probably safe to say that low-cost nanowire TFT technology will have a good chance of becoming a candidate for large-scale, practical applications that include active-matrix organic LED display drivers or even flexible/transparent logic circuits.

## Memory with next-generation nanowires

The small size and excellent control offered by the nanowire system allows it to be used as a platform to study emerging memory concepts. Alternative memory concepts aim to overcome the major limitations of existing electronic memories, i.e. the volatility of Dynamic Random Access Memory (DRAM) and the slow programming speed and limited endurance of flash memory[36]. The ultimate goal is universal memory: high-density memory that can be written and accessed at high speeds for a virtually unlimited number of cycles with data nonvolatility.

Efforts have been broadly focussed on four concepts: ferroelectric, magnetic, resistive and phase-change memory. In ferroelectric memory,

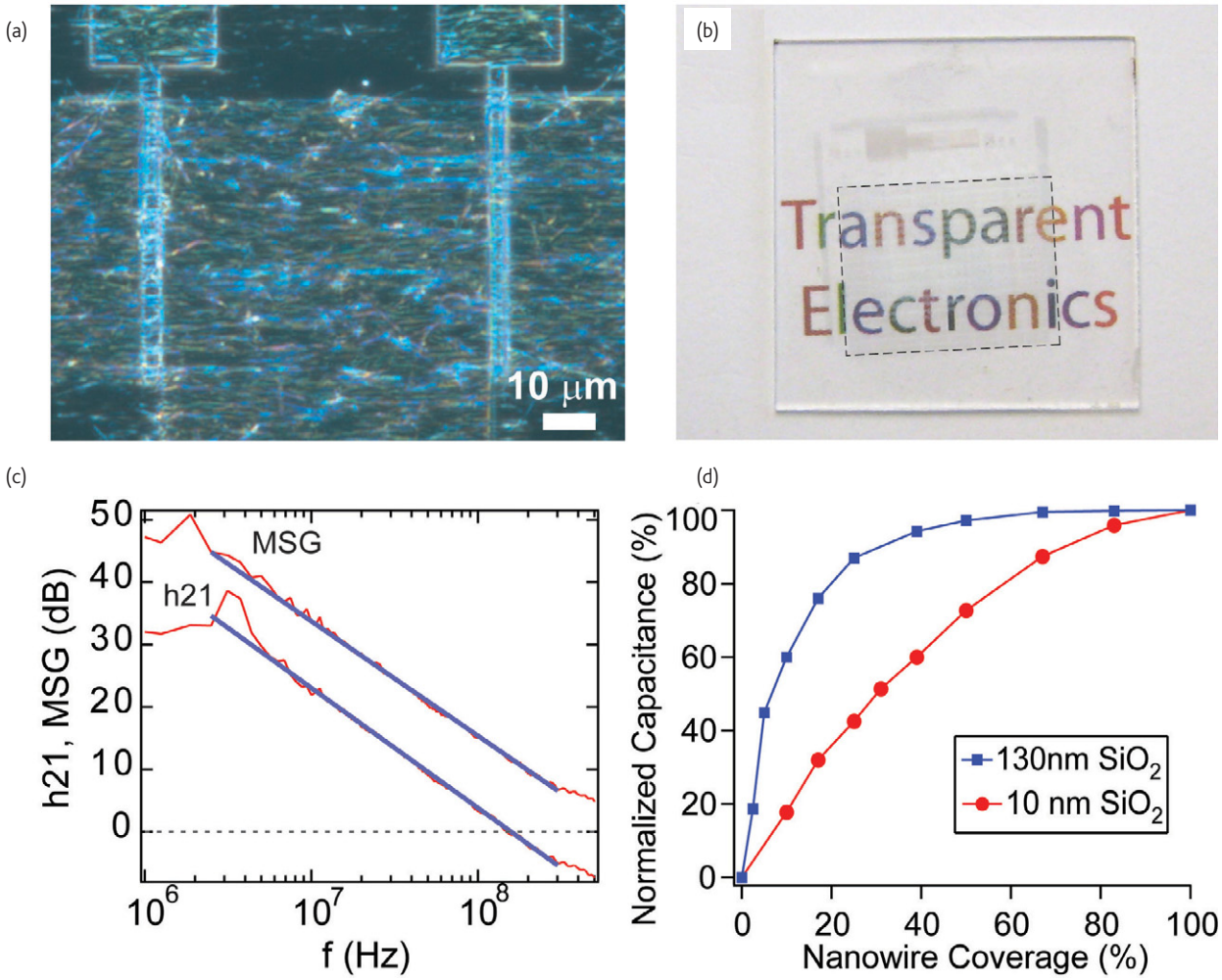


*Fig. 4 Nanowire transparent TFTs. (a) Optical microscopy of a nanowire TFT showing the aligned nanowires as the channel material and the two-finger gate design. (b) Digital photograph of the transparent TFT array on a glass substrate. The device area contains 300 test structures and is marked by a dashed border. (c) Frequency dependence of the current gain ($|h21|^2$) and MSG ($|S21/S12|$) of a transparent nanowire TFT (red lines) and fit using 20 dB roll-off (blue lines). The unity current-gain cut-off frequency $f_T$ was estimated to be 169 MHz and power-gain cut-off frequency $f_{max}$ was estimated to be 700 MHz. (d) Dependence of the nanowire-TFT gate capacitance on nanowire coverage. Reproduced with the permission from Dattoli et al.[35], © 2007 American Chemical Society.*

the polarization states of a ferroelectric material are used to store information, while in magnetic memory, the magnetization states of the material store the information. Ferroelectric memory requires less power, but is quite difficult to scale-down[37,38]. Magnetic memory can be switched rapidly, but requires large currents for programming[39,40]. Resistive memories (RRAMs) rely on the formation of ionic or filament paths between the two terminals and offer small form factor, low power operation and high speed, but questions regarding the reliability of resistance-switching mechanisms still remain[41–44]. Finally, phase-change memory is promising as it is fundamentally scalable, offers high switching speeds, data nonvolatility and random access capability[45].

Chalcogenide-based (Ge–Sb–Te system) phase-change memory, referred to as Ovonic Unified Memory (OUM), is fundamentally different from other semiconductor memories. Information storage is achieved through changes in electrical resistivity/optical reflectivity rather than through manipulation of vanishingly small amounts of charge[45–47]. The reversibly crystalline to amorphous phase transition in Ge–Sb–Te alloys is accomplished by heating and cooling. Phase-change memory utilizing Ge–Sb–Te materials has attracted great attention due to their non-volatile memory properties, fast write/read speeds and low manufacturing costs. Currently, phase-change-based thin-film technology is being used in optical disk storage and is being widely studied for electrical memory applications[48–50]. The major limitations of phase-change memory are the requirements for high scalability, low power consumption and nonvolatility. Often the conventional top-down approach with multiple lithographic and etching steps leads to structural/chemical degradation of phase-change materials, which is detrimental to the above-mentioned requirements. Therefore, despite

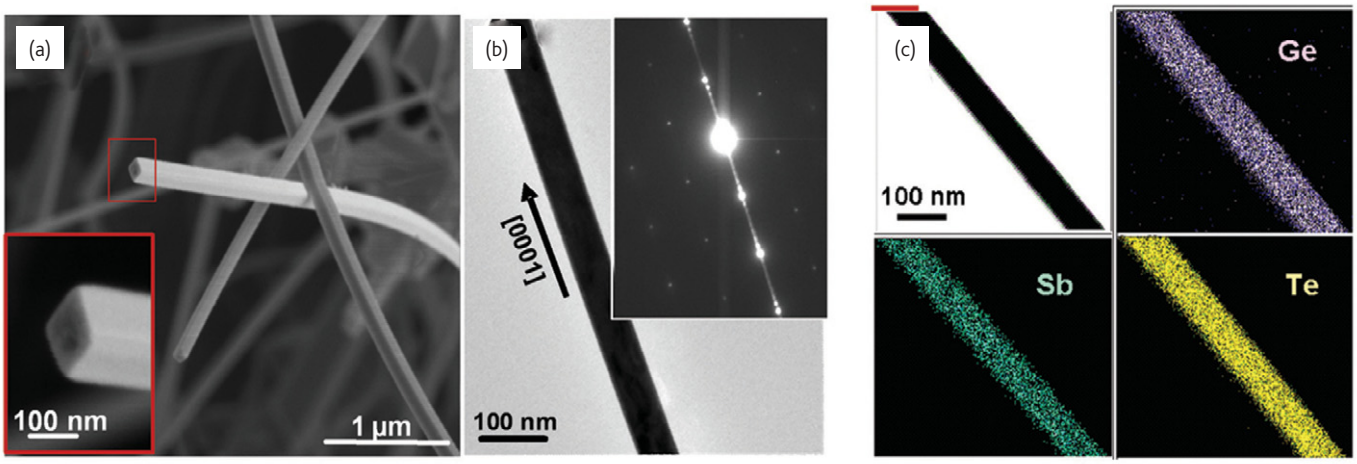


*Fig. 5 (a) Scanning electron microscope image of $Ge_2Sb_2Te_5$ nanowires. The faceted structure of the nanowires implies the single-crystalline nature of as-synthesized phase. (b) Transmission electron microscope and electron diffraction of a $Ge_2Sb_2Te_5$ nanowire showing single-crystalline structure. (c) Energy-dispersive X-ray image showing uniform distribution of elements along the nanowire in the 2:2:5 atomic ratio with no phase segregation. Reproduced with the permission from Li et al.[51], © 2007 Nature Publishing Group.*

many efforts, the intrinsic properties of nanostructured phase-change materials have remained largely unexplored. Self-assembled nanowire-based phase-change memory devices are ideal model systems to gain crucial early insights about the phase-change properties due to their sub-lithographic sizes coupled with facile, etch-free fabrication processes.

Motivated by the challenges, we have successfully synthesized two classes of phase-change nanowires, GeTe and $Ge_2Sb_2Te_5$, by a vapor-phase transport method[51–55]. Synthesis of phase-change nanowires with chemical compositions such as GeTe, $In_2Se_3$, $Sb_2Te_3$, and $Ge_2Sb_2Te_5$ and diameters ranging from 20 to 200 nm has recently been reported by a few groups[56–59]. The structure and chemical composition of $Ge_2Sb_2Te_5$ nanowires, obtained from electron microscopy and energy-dispersive spectroscopy, show a single-crystalline structure with desired chemical compositions and no evidence of phase segregation of chemical constituents (Fig. 5a–c)[51].

Single-nanowire devices show reversible memory switching behavior with extremely low writing currents. Current–voltage (I–V) measurements of a 60 nm thick, crystalline nanowire device display ohmic behavior with low resistance (Fig. 6a)[51]. The DC I–V measurements of a nanowire in an amorphous state obtained by applying a current pulse shows much higher resistance at low applied bias and by a clear threshold switching event at high fields, followed by an amorphous to crystalline phase change with Joule heating (Fig. 6a)[51]. The 'reset' (amorphization) currents obtained for nanowire devices are significantly lower than those of product-level phase-change memory devices achieved in the semiconductor industry. Programming characteristics obtained by measuring the resistance (R) change as a function of writing/erasing current (I) pulse amplitude (Fig. 6b)[51] show two distinct memory states: highly resistive 'reset' amorphous and low resistive 'set' crystalline states with typical resistance ratios $>10^2$. For a 60 nm device, switching speeds as low as ~50 ns can be obtained without compromising the resistance of the final recrystallized state (Fig. 6c). The operation of the device was maintained without failure for up to $>10^5$ cycles performed with alternating write/read/erase/read pulses (Fig. 6d)[51]. Therefore, based on the electrical switching data, it is apparent that $Ge_2Sb_2Te_5$ nanowires can be considered as fast, reversible and reliable memory devices. Remarkably, the size-dependent memory switching behavior of $Ge_2Sb_2Te_5$ nanowires shows that amorphization current decreases systematically by scaling-down the nanowire diameter (Fig. 6e); currents as low as 0.16 mA were achieved for 30 nm thick nanowire, a drastic decrease from 1.5 mA for a 200 nm nanowire[51]. At the same time nanowire resistance-change reveals that rapid recrystallization occurs for thinner nanowires with reduction in data retention times and activation energies ($E_a$) as a function of the nanowire thickness (Fig. 6f). For example, at 80°C, a data retention time and an $E_a$ of ~3.0 years and 1.98 eV, respectively, were obtained for a 30 nm nanowire, a large drop from ~1800 years and 2.34 eV for a 200 nm nanowire. All tested nanowires displayed extremely long data retention at room temperature (>100,000 years!). The observed size-dependent amorphization and recrystallization in nanowires can be attributed to suppression of phase-transition temperatures with size reduction owing to the increase in the surface-to-volume ratio of atoms as suggested by experiments and from the thermodynamic theory of materials in confined geometries[51].

The memory switching characteristics also depend on chemical composition. Lower energy is required to switch $Ge_2Sb_2Te_5$ nanowires compared to GeTe due to their lower phase-change temperatures and higher resistivity[54,55]. Utilizing this property, we assembled novel heterostructured phase-change multistate memory devices to enable memory capacity to scale with $3^N$ rather than the $2^N$ found for conventional binary-logic devices[20]. We synthesized core/shell nanowires by depositing GeTe shell onto $Ge_2Sb_2Te_5$

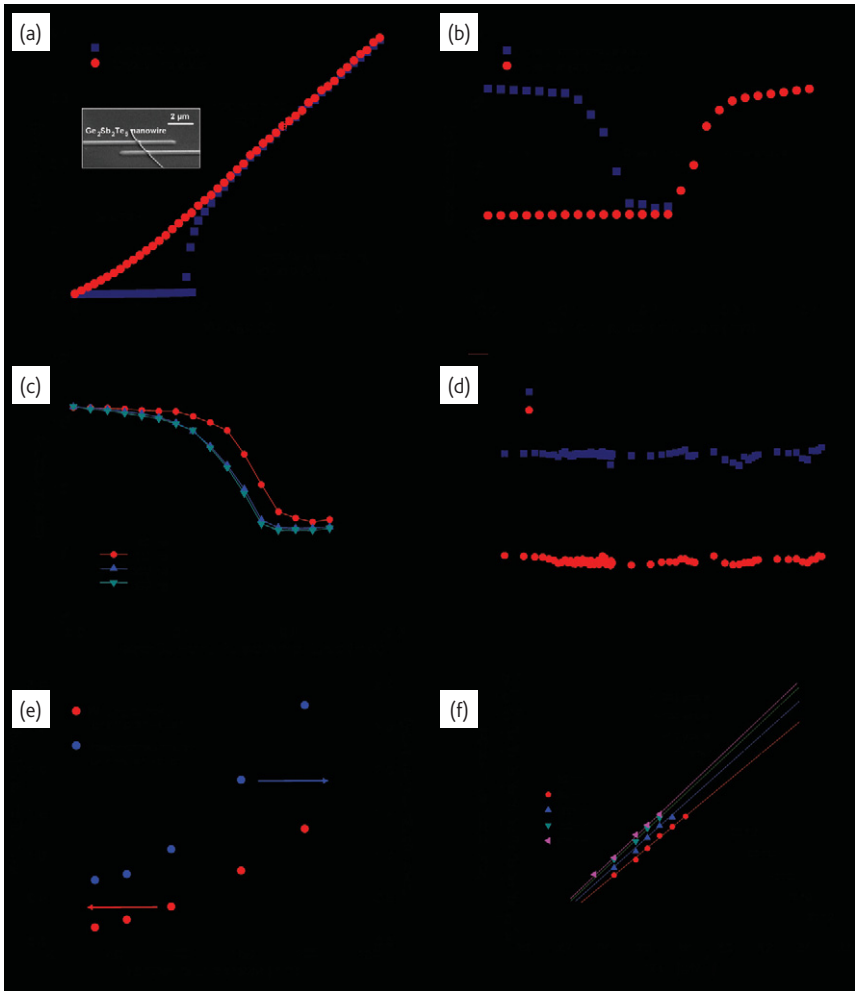


*Fig. 6 Electrical switching data of single $Ge_2Sb_2Te_5$ nanowire devices. (a) I–V characteristics of a 60 nm $Ge_2Sb_2Te_5$ nanowire in different physical states: amorphous (squares) and crystalline (circles). (b) Resistance change in the $Ge_2Sb_2Te_5$ nanowire memory device as a function of writing pulses of varying current amplitudes (programming curves, 100 ns for amorphous state and 300 ns for crystalline state) obtained for initially amorphous (blue squares) and crystalline (red circles) phases. The crystalline and amorphous phase regions are clearly demarcated. (c) Pulse-duration-dependent switching data showing switching in 50 ns. (d) Endurance-cycling test for a 60 nm $Ge_2Sb_2Te_5$ nanowire device. The write/read/erase/read pulse sequences are applied continuously. (e) Size-dependent writing current data showing dramatic reduction in switching current and power with smaller size. (f) Size-dependent recrystallization kinetics showing reduction in activation energy with decreasing size. However, even a 30 nm nanowire shows a data retention of 100,000 years. Reproduced with the permission from Lee et al.[51], © 2007 Nature Publishing Group.*

core nanowires with good control over their compositions and interfaces (Fig. 7a–c)[55]. Significantly, core/shell nanowires display multistate memory switching upon application of an electrical pulse; two-step threshold switching in DC I–V sweep; and three distinct electronic states of low, intermediate and high resistances, assigned as data 0, 1, and 2 (Fig. 7d,e). The observed multiple electronic states represent different structural states of the constituents, resulting from sequential amorphous/crystalline phase change in the core/shell. The nonbinary data storage realized in free-standing core/shell nanowires will allow data storage at very high densities and make possible practical devices configured from only a few nanowires without the need to develop complex schemes to assemble large quantities of nanowires in addition to enabling fundamental studies of novel materials and phase-change phenomena. These studies suggest that phase-change memory nanowires hold great promise for nonvolatile, ultrahigh-density memory and may represent the ultimate size-limit in exploring current-induced phase transitions in defect-free systems.

## The empire strikes back

Bottom-up nanowires for high-performance electronic devices are, without any doubt, intriguing. The advantages such as a vertical nanowire FETs as well as the possibility of III–V integration on Si are significant prospective milestones. However, the practical application of these device concepts requires much engineering effort to address the manufacturability and reliability problems, particularly for

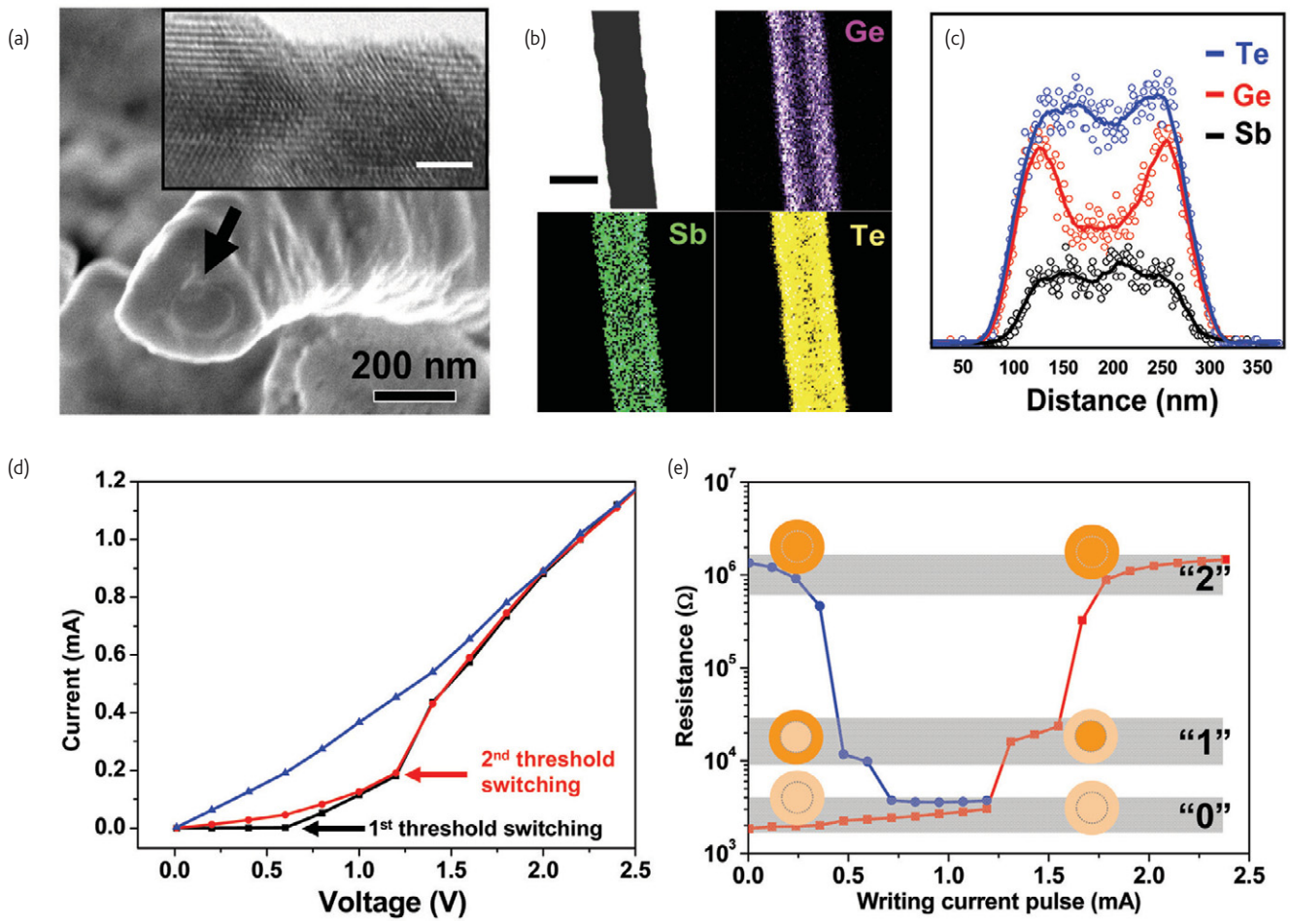


*Fig. 7 Structural characterization and electrical behavior of $Ge_2Sb_2Te_5$/GeTe core/shell phase-change nanowire memory device. (a) Scanning electron microscope image of focussed ion beam cross-sectioned $Ge_2Sb_2Te_5$/GeTe-core/shell nanowire. Clear interface between core and shell regions is visible, as denoted by the arrow. Inset is a high-resolution transmission electron microscope image of a polycrystalline GeTe shell region. Scale bar: 2 nm. (b) Elemental mapping image showing spatial distribution of Ge, Sb and Te in a core/shell nanowire. Scale bar: 200 nm. (c) Cross-sectional energy-dispersive spectroscopy line-scan profile of the nanowire in (b), (d) DC I–V sweep characteristics of a 200 nm core/shell nanowire device showing electrical behavior of fully crystalline (blue), partially amorphized (red) and fully amorphized (black). The two-step threshold switching (marked by arrows) is clearly resolved for a fully amorphized nanowire (black: amorphization current pulse, 2.0 mA, 100 ns). (e) Programming data: variation of resistance of the core/shell nanowire device as a function of current pulses with varying amplitudes. Pulse durations are 100 ns for amorphization and 300 ns for crystallization. The three different resistive states (low for '0', intermediate for '1', and high for '2') realized with application of current pulses are highlighted (gray bands). The schematics represent the cross-section of the core/shell nanowire at each stage of transition. Reproduced with the permission from Jung et al.[55], © 2008 American Chemical Society.*

high-performance devices based on individual nanowires with deep sub-100 nm channel lengths. Without addressing these lingering questions, research in academia over the past 10 years may be just spectacular demonstrations of novel chemical and physical phenomena. On one hand, the end of the semiconductor roadmap is inevitable and CMOS engineers are searching for new materials beyond Si and $SiO_2$ (e.g. $HfO_2$), and architectures to keep pace with the requirements of ever-shrinking Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). As a result, major stakeholders in the semiconductor industry have shown interest in utilizing nanowire-based FETs for practical devices. Recently, a few groups have shown that one can rationally position and fabricate single wrap-gated FETs with vertically oriented nanowires[60–62]. IBM Rüschlikon, Switzerland, even demonstrated an impact ionization nanowire FET concept with subthreshold swings of ~5 mV/decade, beating the fundamental thermodynamic limit kT/q of 26 mV (thermal voltage) or the minimum subthreshold slope of 60 mV/decade at room temperature (Fig. 8)[63]. This intriguing vertical nanowire concept potentially offers also an ultimately small footprint for FETs. However, results on vertical Si and InAs nanowire FETs show that vertical integration comes with a price. Essentially all CMOS processes are optimized for planar thin films. The third dimension leads to problems such as contact resistance and parasitic capacitance. In addition, vertically grown nanowires are not defect free. Givargizov[64], a pioneer in the days of the semiconducting 'whisker', stated a rule of thumb that lowering the VLS growth temperature more than one-third below the melting

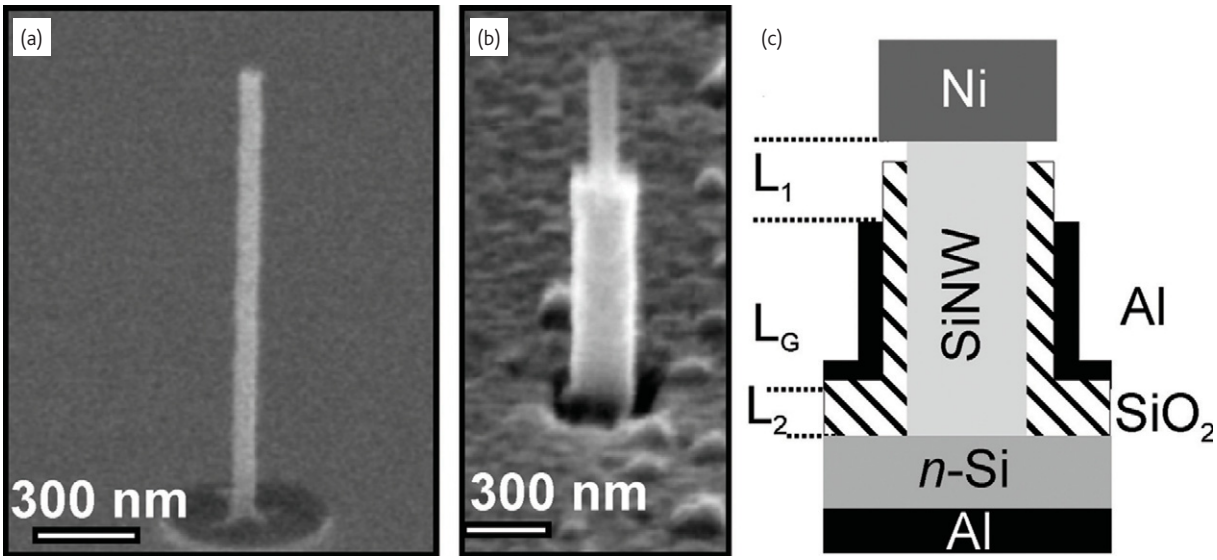


*Fig. 8 Processing of vertical Si nanowire impact ionization FETs. (a) 60 nm diameter Si nanowire covered with 25 nm $SiO_2$ gate dielectric. (b) Wire with wrap-gate. (c) Schematic of the surround-gated transistor showing the gate length LG and ungated regions L1 (200 nm) and L2 (25 nm). Positive or negative gate bias on this reverse biased 'pin' diode defines if electrons (L1) or holes (L2) are enriched at LG and avalanche breakdown occurs over the ungated nanowire parts. Reproduced with the permission from Bjoerk et al.[60], © 2007 American Institute of Physics.*

point of the semiconductor usually leads to defects in the nanowire structures.

On the other hand, instead of relying on bottom-up grown nanowires, CMOS researchers are now looking into solving the manufacturability and reliability problems associated with nanowires with top-down engineering skills. As early as 1993, when silicon nanostructures for photonics applications caught the attention of researchers, the Pease group at Stanford[65–67] realized that Si can be scaled down to the sub-5 nm regime with high precision using stress-limited oxidation (Fig. 9). During Si oxidation processes, the oxide is pushed further out as the oxidation of the Si surface progresses. This process is self-limiting at temperatures below 950°C where the high viscosity of the $SiO_2$ makes this radial plastic deformation of the outer oxide layers of the Si nanowire difficult and as a result a large normal stress is generated at the Si–$SiO_2$ interface of the nanowire. Fifteen years later, the Kwong group[68] at the Institute of Microelectronics, Singapore, utilized the concept of stress-limited oxidation to fabricate NMOS and PMOS FETs with diameters of 5 nm and less with almost ideal subthreshold swings of 65 mV/decade (Fig. 10). Samsung[69] followed and demonstrated nanowire FETs on the same scale with gate lengths of 30 nm. The diameter of these top-down fabricated silicon nanowires of sub-5 nm diameter is on a length scale that is barely accessible with bottom-up grown silicon nanowires[70].

An ongoing discussion with nanowire FETs is the charge carrier mobilities which are used to benchmark FETs. Extracting the mobility values from planar devices is a straightforward process. However, nanowire mobilities are usually derived from bottom-gated structures where the gate oxide capacitance cannot be quantified and the nanowire FETs are often operated in the depletion mode, resulting on non-ideal FET characteristics[71,72]. Most papers report current

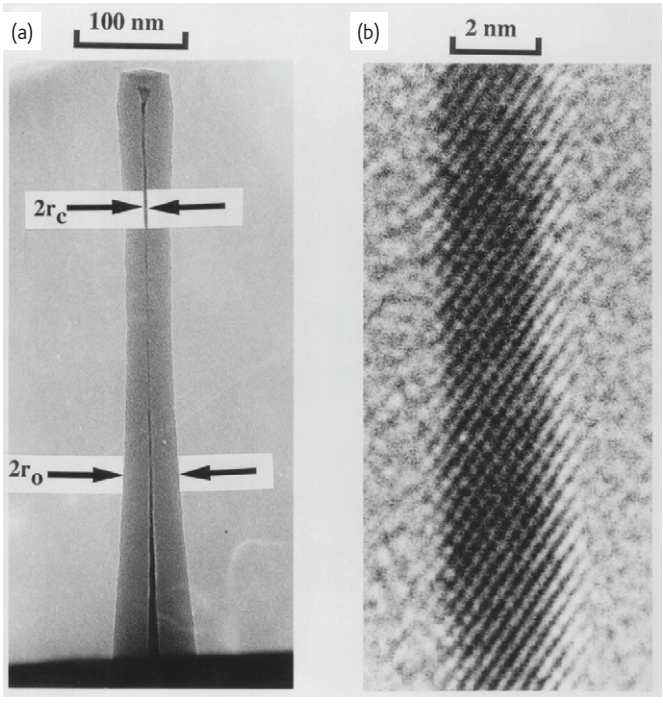


*Fig. 9 Stress-limited oxidation of Si. (a) Transmission electron micrograph of an oxidized Si nanocolumn (875°C for 10 h) showing the general shape of a typical column. The inner Si core has already reached its limiting dimensions. (b) A high-resolution lattice image of the inner Si core (2 nm in diameter) when the column has reached the self-limiting regime at 875°C. Reproduced with the permission from Liu et al.[65]. © 1994 American Institute of Physics*

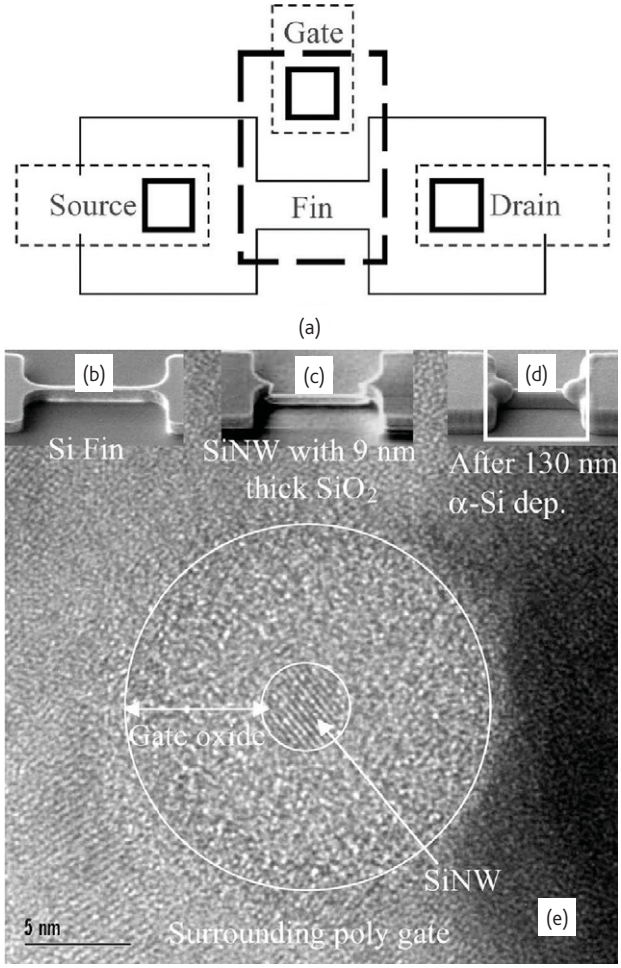


*Fig. 10 Lateral wrap-gated nanowire FET. (a) Layout of the masking layers used in the fabrication process. (b) Tilt view scanning electron microscope image of 1000 nm long, 50 nm wide and 200 nm tall Si fins after top silicon etch with ends of the fin connected to S/D pads. (c) Si nanowire after 9 nm thick $SiO_2$ deposition. (d) Si nanowire after 9 nm thick gate oxide and 130 nm α-Si deposition. The drawn rectangle shows the gate pattern schematic. (e) Transmission electron microscope image perpendicular to the wire of a 200 nm long nanowire showing a circular 4 nm thick wire 9 nm oxide with full coverage by α-Si from all sides. Reproduced with the permission from Namatsu et al.[67], © 2006 IEEE.*

per unit length values (e.g. mA/μm) using the circumference of the nanowire, which is reasonable as long as the nanowire diameter is large and the charge is located at the surface. With small diameters, however, one can expect bulk inversion so the charge is at the center of the nanowire and dividing by the diameter may be more realistic. Most recently, IBM researchers shed some light on this issue and reported a detailed method to obtain mobility values on FETs with VLS-grown nanowires. In this recent paper Cohen et al.[73] evaluated the effect of edge roughness of bottom-up grown nanowires in comparison to etched nanowires. They observed that the mobility of thick nanowires FETs compare well to planar MOSFETs but gradually decreased with sub-10 nm nanowire diameters. At the same time, a second IBM team reported the first direct capacitance measurements

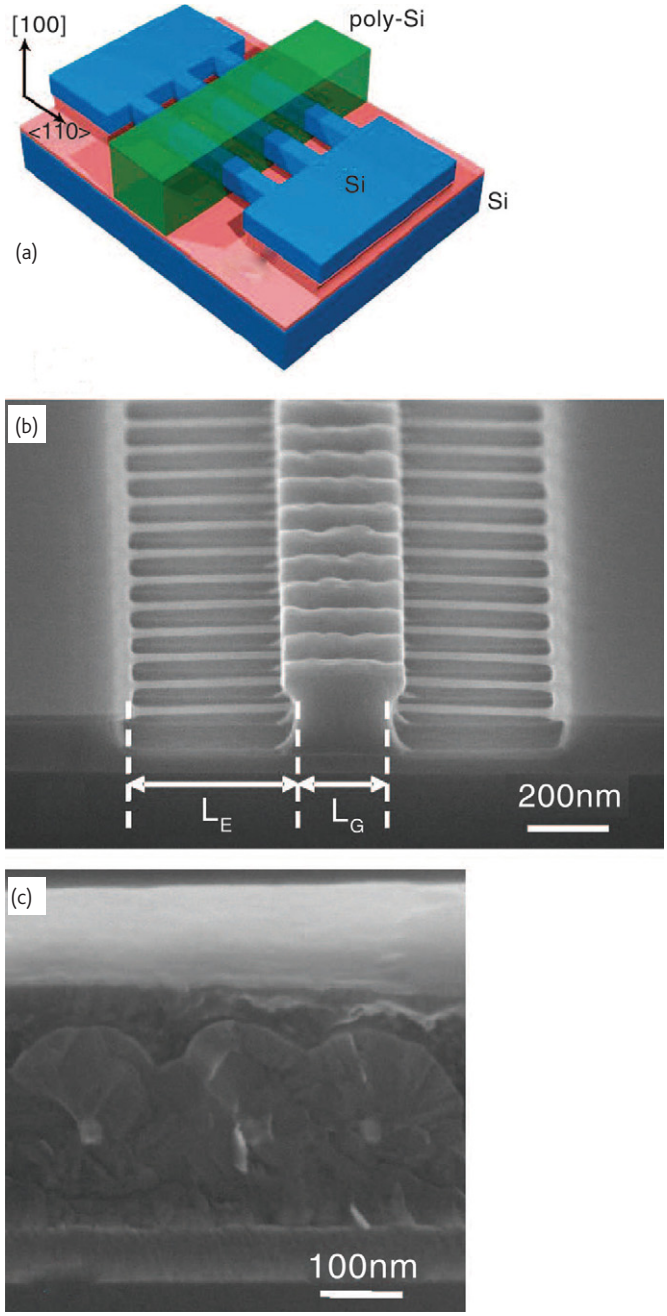


*Fig. 11 Capacitance measurements with arrays of nanowires. (a) Schematic of the final Si nanowire array FET structure on (100) Si wafers with the wires oriented along the <110> direction. (b) A side-view scanning electron micrograph of the final structure after gate formation. The gate length LG 250 nm and the extension region length LE 375 nm for this structure. (c) A cross-sectional scanning electron micrograph of the Si nanowires with wrap-around poly Si gate. Reproduced with the permission from Cohen et al.[73], © 2008 American Chemical Society.*

and accurate mobility measurements of top-down fabricated silicon nanowires (Fig. 11). The etched nanowires in this work are bound by a combination of roughly comparable admixtures of (100) and (110) Si surfaces. Surprisingly, the comparison of FETs operating in

the surface inversion regime between intrinsic Si nanowire with ~20 nm diameter and bulk Si showed that the nanowire carrier mobilities appear to be closer to those of the surface orientation that offers a lower mobility for the specific carrier type[74]. For example the electron mobilities in intrinsic nanowires are closer to the lower mobility values for (110) Si compared to the higher electron mobility with (100) Si surfaces. The results of the IBM papers indicate that both bottom-up as well as top-down Si nanowire FETs have comparable electron mobilities.

It might appear that CMOS is advantageous for utilizing nanowires for assembling practical devices. This is only true for Si. The beauty of the bottom-up approach is the ability to create structures that are impractical for top-down fabrication such as novel heterostructures in various geometries combining otherwise incompatible materials, which can most likely never be realized with planar systems due to large lattice mismatches. One dream would be to integrate III–V semiconductors on Si with vertical growth of InP and GaAs nanowires on Si as demonstrated by Philips[75] and Samuelson's groups[76], respectively. It remains to be seen if the holy grail of bottom-up technology, such as III–V integration on Si or highly promising core/shell nanowires[17] can be further developed to an industrially relevant process. In the meantime, there are plenty of science and engineering challenges and novel opportunities that remain to be explored by utilizing bottom-up and top-down nanowire devices, which will continue to drive research in this exciting area. nt

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